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An 89dB Dynamic Range CMOS Image Sensor with Dual Transfer Gate Pixel

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Abstract

This paper presents a 1 Megapixel CMOS image sensor which applies a dual charge transfer (dual-TX) scheme in the pixel to achieve a high dynamic range. The prototype sensor uses analog outputs and operates at maximum 20fps in rolling shutter. The sensor achieves 3.3e- temporal noise and 99Ke- full well capacity with 10μm pixel pitch.

1: Introduction

High sensitivity and wide dynamic range are key requirements for many imaging applications. However, to design a CMOS image sensor with very low read noise combined with high full well charge (FWC) is not straightforward. In a typical pinned photodiode (PPD) 4T pixel structure, the dominating noise source after correlated double sampling (CDS) is the source follower noise (thermal, 1/f and RTS noise). In order to lower the noise, the pixel conversion gain needs to be designed as high as possible, which limits the full well capacity (FWC).

Therefore, special techniques are required to achieve low noise and high dynamic range at the same time. One example is by modulating the exposure time, e.g. multiple exposures or multiple slopes (conditional/partial reset) [1]. However, this type of method introduces motion distortion artifacts because the exposure happens at different time in one frame. In addition, the signal-noise ratio (SNR) becomes discontinuous at the transition points between different integration times. In order to extend the FWC of the PPD, e.g. in a small pixel pitch, the lateral overflow integration capacitor (LOFIC) concept can be used by partially open the TX transistor so that the over-saturated charges overflow to a separate capacitor [2]. But this overflow path also relies on the TX transistor threshold voltage which normally has large variance, and partially opened TX transistor during exposure could introduce additional dark current source resulting higher dark current shot noise. If the FWC of PPD is sufficient, one has to increases the FWC of the FD while keeping the conversion gain high enough. One solution is by sequentially partial transferring the charge from the PPD [3]. In this case, the gate voltage bias of the transfer transistor (TX) is modulated to control the maximum amount of charge being transferred in each cycle. But using this method results in complex driving circuitry and requires fast readout. In addition, the TX transistor threshold variation causes pixel-to-pixel uniformity in different transfers. Another solution is the dual-gain pixel [4], in which the pixel conversion gain can be changed by attaching a switchable capacitance to the floating diffusion (FD). In this case, two charge transfer steps are required, one with high conversion gain and one with lower gain. In addition, the readout chain has to be optimized as well in order to achieve low read noise meanwhile not limiting the pixel FWC, to solve this problem, two separate readout chains with different gain settings are designed inside each pixel pitch in [5].

In this paper, we present a new pixel architecture that is capable to achieve low noise and HDR through implementing a dual-TX structure. This method does not rely on the TX transistor threshold and the complete charge is transferred in one operation (consists of four steps).

2: Dual-transfer gate pixel

Figure 1 explains the basic working principle of the dual-TX scheme in case of over-saturation. There are two FDs (thus, two different conversion gains) in each pixel, and each FD is attached to its own transfer transistor. The complete charge transfer phase is done by overlapping the two TX-on phase. The difference in FD capacitances (thus conversion gains) can be achieved by sizing the transfer transistor or adding separate capacitance. In the figure, FD1 attached to TX1 transistor represents the FD with higher conversion gain, and FD2 attached to TX2 transistor is larger and capable to accommodate all charges transferred from the PPD.

During exposure, both TX1 and TX2 transistor is switched off, leaving the photon-generated electrons accumulated in the PPD. During charge transfer, TX1 transistor is first on to transfer the charges to FD1, in case of over-saturation,

charge sharing happens as shown below. Afterwards, TX2 is switched on, allowing an overlap period when both TX1 and TX2 are switched on. Because FD2 has a much larger capacitance, all remaining charges in the PPD will flow to FD2. After then TX1 is switched off, the charge under TX1 gate will be dumped to FD2 as well. In the end, TX2 is switched off and the complete charge transfer operation is completed. In case of low illumination, all charges will be transferred to FD1 and no signal is seen from FD2. In case of high illumination, the charges are transferred to both FD1 and FD2. The complete charge transfer is completed in one operation using this technique.

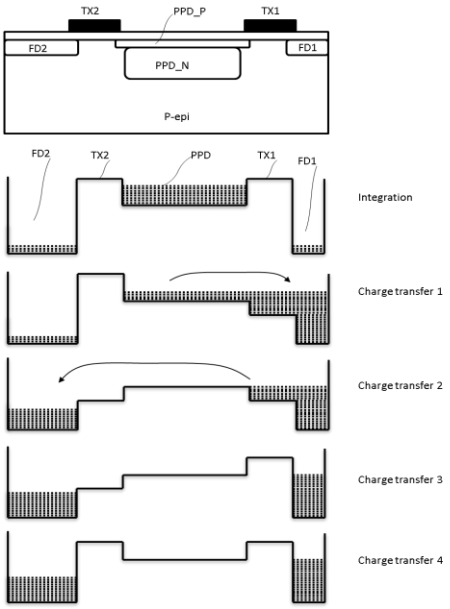

Figure 1: Dual-transfer concept

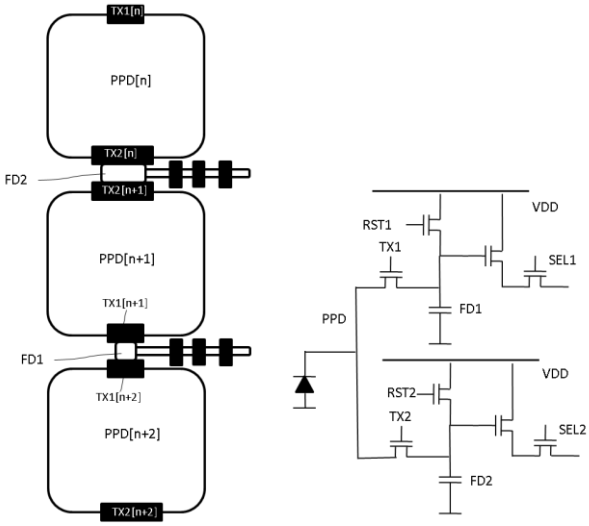

Figure 2: Baseline pixel architecture

Figure 2 shows a pixel example and its layout. In each pixel, two separate output chains using TX1 or TX2 are included, but in layout, they can be shared between pixels on top of each other as shown. This pixel can operate in several modes includes:

- Normal 4T mode: standard 4T timing except the odd and even rows are readout from the output chain located in the opposite side of the PPD. The charge transfer is done using only one TX for all pixels, either TX1 or TX2. In this case, the pixel dynamic range is the same independent whether TX1 or TX2 is used and determined by the FD voltage swing and the SF noise. But the temporal noise is lower when TX1 is used and FWC is higher if TX2 is used.
- HDR mode: dual-transfer scheme is applied in this mode. For all pixels in each row, there are two signals being readout using from both top and bottom chain, through TX1 and TX2 transistor. The signal with lower conversion can be amplified (depends the ratio of FD1/FD2) and being added to the high gain signal off-chip and reconstruct the final HDR image.
- Charge-binning mode: If higher sensitivity is desired, the sensor y-resolution can be sacrificed and the PPDs in both odd/even row pixels are readout simultaneously through TX1. In this case, the pixel SNR is doubled because of charge binning.

Figure 3 shows another pixel example to where this scheme can be applied. The readout timing is included as well. As shown, before readout, the reset transistor is off while HDR switch is on. FD2 and FD1 are shorted together at this moment. This level on FDs is then sampled as the reset value for low gain channel. After then, HDR is off, the level on FD1 is sampled as reset level for high gain channel. Then the overlapping charge transfer is used to transfer all changes to both FD1 and FD2. Sampling the signal on FD1 as the signal level of high gain, and then closing HDR again to combine the charges on both FD1 and FD2, this value can be taken as signal of high gain path. The advantage of this pixel is that the total charge signal is available in the low-gain path, instead of only part of them as in the pixel of figure 2.

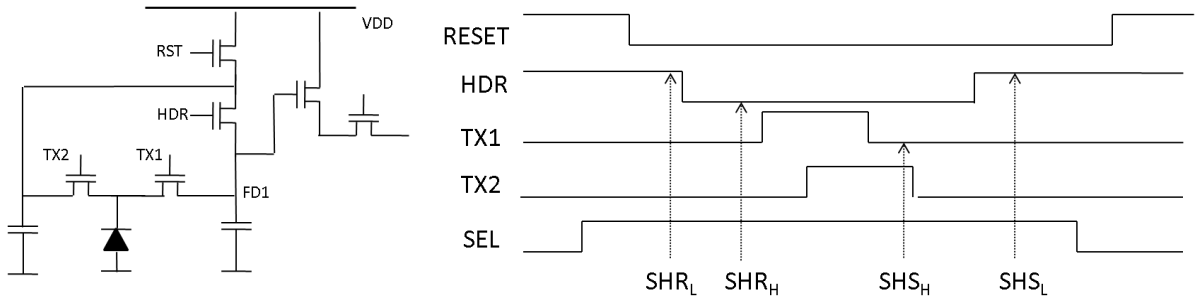

Figure 3: 6T HDR pixel architecture and timing during readout

3: Prototype sensor design

A 1Megapixel CMOS image sensor using proposed HDR scheme is designed and fabricated in TowerJazz 0.18μm process. Figure 4 shows the sensor architecture, the pixel array resolution is 1024x1024 with pixel pitch of 10um. Two gain paths are designed in each pixel pitch in order to further optimize the full dynamic range and to minimize the noise contribution from the analog chain. The gain of each path can be set individually.

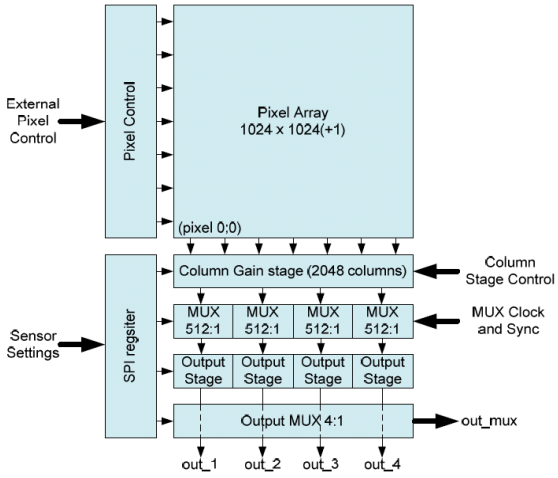

Figure 4: Sensor architecture

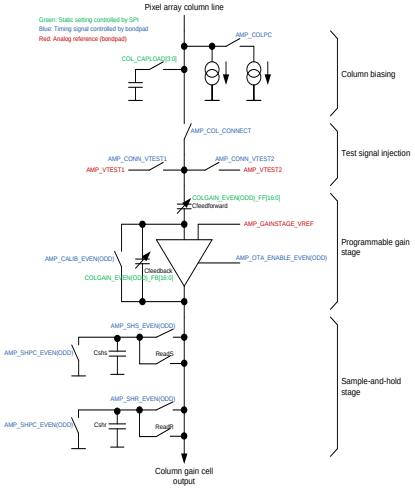

Figure 5: Column gain stage block diagram

Figure 5 shows a detailed block diagram of a single column gain cell. There are two identical cells in each pixel pitch. Besides the gain amplifier, the column biasing, test signal injection and sample-and-hold stage is included in this block as well. The column biasing sets the bias conditions for the source follower in the pixel. Four extra capacitances can be added to the column line to reduce the source follower noise by limiting the bandwidth. A test signal injection possibility is foreseen in the column gain stage in order to measure the signal path transfer characteristics. The gain amplifier applies a programmable gain of 1x up to 16x to the pixel signal. The gain settings can be controlled separately for the 'high' and 'low' gain output columns. Each column sample-and-hold stage contains two sample-and-hold capacitors. One is used to store the amplifier calibration level, the other one is used to store the integrated signal level. The difference between both levels is the actual integrated pixel value, after the gain applied in the column. After the column gain stage, all columns in a quarter of the full array are sequentially select by the multiplexer. The output of the column multiplexers are four high-speed analog signals, which serves as the input of the output stage blocks as shown in Figure 4. The output stage performs CDS and a programmable offset is added to the signal. The sensor output is a fully differential analog signal.

4: Sensor characterization result

Figure 6 shows the response curve measured from the prototype sensor, the pixel type and timing is as the one shown in figure 3. The column gain for high gain channel s set to x3.25 and for low gain channel is 1.13x. The gain setting is tuned to allow a smooth SNR transition from the high gain to low gain channel. Further increases the gain setting for the high gain channel can further lower temporal noise, however at the cost of SNR drop at crossing point. Figure 7 is the photon transfer curve measured with the same setting. As shown, the saturation level for the FD1 channel is close to 5ke-, and for FD2 channel is 99ke-. The dark temporal noise measured from the high gain channel is 3.34e-. The combined dynamic range is close to 90dB. At the transition point, the SNR drops from 39dB to 36.5dB by switching from high gain to low gain channel. Table 1 shows the overall sensor characterizations results and figure 8 shows a test image from both channels.

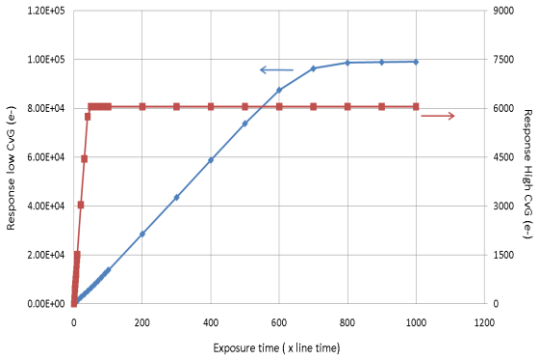

Figure 6: Response measurement

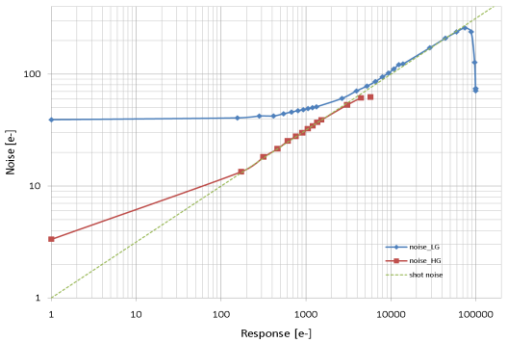

Figure 7: PTC curves

Parameters	Low gain channel	High gain channel	unit
Conversion gain	12.2	78	uV/e-
FWC	99000	5200	e-
Noise	39	3.3	e-
Dynamic range	89.54		dB
Dark current @ room T	80		e-/s
Lag	<0.1		%
PRNU	0.4	0.68	%, rms

Table 1: Sensor characterization table

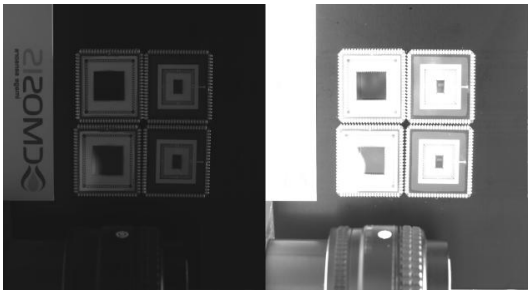

Figure 8: test image (left: low gain channel, right: high gain channel)

5: Conclusion

In this paper, we present a HDR method with a pixel using pulsed overlapping charge transfer by 2 TX transistors. The sensor dynamic range can be increased significantly if the limiting factor is the FD or readout circuitry (i.e. the PPD has large FWC). A prototype sensor is fabricated and proved the pixel concept; 89dB dynamic range is achieved with 3.3e-noise.

Acknowledgement

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References

[1]: J. Solhusvik et al., "A 1280 × 960 3.75 µm pixel CMOS imager with Triple Exposure HDR," IISW 2009.
[2]: S. Sugawa et al., “A 100dB dynamic range CMOS image sensor using a lateral overflow integration capacitor”, ISSCC 2005.
[3]: S.Shafie et al.,” Non-Linearity in Wide Dynamic Range CMOS Image Sensors Utilizing a Partial Charge Transfer Technique” Sensors 2009, Vol.9, p 9452-9467
[4]: X.Li “MOSFET Modulated Dual Conversion Gain CMOS Image Sensors”, Ph.D Thesis, Boise State University, Nov 2008.
[5]: B.Fowler et al.,”Wide dynamic range low light level CMOS image sensor”, Fairchild imaging, IISW 2009